



CoreLink™ SSE-100 Subsystem Software Developer Errata Notice

This document contains all errata known at the date of issue, in releases up to, and including, revision r0p1.

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If you have comments on content then send an e-mail to errata@arm.com giving:

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- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

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Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

- | | |
|--------------------------|--|
| Category A | A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications. |
| Category A (Rare) | A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage. |
| Category B | A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications. |
| Category B (Rare) | A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage. |
| Category C | A minor error. |

Change control

Errata are listed in this section if they are new to the document, or marked as “updated” if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The errata summary table on page 7 identifies errata that have been fixed in each product revision.

11-Dec-2017: Changes in document version 2.0

ID	Status	Area	Cat	Summary of erratum
1025514	New	Programmer	CatC	Wrong value of Peripheral ID (PID3) register
1027534	New	Programmer	CatC	Error response from eFlash lost upon turning off eFlash Cache

05-Oct-2016: Changes in document version 1.0

ID	Status	Area	Cat	Summary of erratum
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No errata in this document version.

Errata summary table

The errata associated with this product affect product versions as below.

ID	Cat	Summary	Found in versions	Fixed in version
1025514	CatC	Wrong value of Peripheral ID (PID3) register	r0p0	r0p1
1027534	CatC	Error response from eFlash lost upon turning off eFlash Cache	r0p0	Open

Errata descriptions

Category A

There are no errata in this category.

Category A (rare)

There are no errata in this category.

Category B

There are no errata in this category.

Category B (rare)

There are no errata in this category.

Category C

1025514

Wrong value of Peripheral ID (PID3) register

Status

Affects: CG061 Arm CoreLink SSE-100 Subsystem

Fault type: System Category C.

Fault Status: Present in r0p0. Fixed in r0p1.

Description

The SSE-100 has integrated timers with read-only identification registers. The Software uses these registers to identify the peripheral, and the revision of the peripheral. After Cold reset, the PID3 register of the timers does not have a proper value until the first register read.

To trigger the erratum, the Software reads the PID3 register before reading any other timer register.

Configurations affected

This erratum affects system configurations that meet all the following requirements:

- All SSE-100 configurations

Conditions

1. Reading the PID3 timer register before accessing other timer registers.

Implications

This erratum might be result in the Software failing to properly identify timer peripherals in the SSE-100 subsystem.

Workaround

After Cold reset, read a timer register other than the PID3 register.

1027534

Error response from eFlash lost upon turning off eFlash Cache

Status

Affects: CG061 Arm CoreLink SSE-100 Subsystem

Fault type: System Category C.

Fault Status: Present in r0p0.

Description

The SSE-100 has an integrated eFlash cache to reduce eFlash accesses. The eFlash is typically used for code storage, therefore it acts as an instruction cache. If the prefetcher option of the eFlash cache is enabled (where the Configuration and Control register SET_PREFETCH bitfield is set to 1), this erratum might result in a Use Fault exception of the Cortex-M3 instead of a Bus Fault exception, when the instruction fetch from the eFlash ends with an error. If the eFlash is used for data storage, this erratum might result in reading incorrect data from the eFlash without getting a bus error notification about erroneous data.

To trigger the erratum, use the prefetcher option of eFlash cache. The software running on Cortex-M3 disables the cache (changes Configuration and Control register Enable bitfield to 1'b0) while there is an ongoing prefetch transaction. If the prefetch transaction is unsuccessful (where the eFlash sends an error response) and there is a cache hit to the prefetch data when prefetch operation is ongoing, the Cortex-M3 processor receives erroneous data without an error notification (with the response okay and not a response error). If the erroneous transfer is a code fetch, this erratum might result in a Use Fault exception instead of a Bus Fault exception that is triggered by the Cortex-M3. If the erroneous transfer is data read, this erratum results in wrong data received without an error notification.

This situation can happen only when software is writing or erasing the eFlash without disabling the eFlash Cache. This behaviour is a source of data inconsistency between eFlash and eFlash Cache and should be avoided. It is expected to disable the eFlash Cache before the write or erase operation of the eFlash starts.

Configurations affected

This erratum affects system configurations that meet all the following requirements:

- eFlash Cache is enabled (CCR.EN = 1).
- prefetcher in eFlash Cache is enabled (CCR.SET_PREFETCH = 1).

Conditions

1. eFlash write or erase is ongoing.
2. Prefetcher in eFlash Cache is enabled.
3. Disabling the eFlash Cache when the prefetch transaction is in progress.
4. Prefetch transaction is addressing an eFlash bank where a write or erase operation is ongoing.
5. Prefetch transaction results in unsuccessful transfer (error response).
6. Access to the prefetched address when a prefetch is ongoing.

Implications

When an erroneous transfer is a code fetch, this erratum might result in a Use Fault exception of the Cortex-M3 while a Bus Fault exception would be the proper response.

When erroneous transfer is a data read, this erratum results in an incorrect data read from the eFlash without an error indication to the initiator of the transfer.

Workaround

The issue should not happen during normal operation as it is expected to not try to read the eFlash while erasing or writing the eFlash. The prefetcher option should be disabled or the eFlash read might result in an erroneous transfer.